A very low distortion SiGe BiCMOS Down Converter for W-CDMA Applications

Daisuke Watanabe*, Ikuo Imanishi*, Junji Itoh*, Toshifumi Nakatani**, Takaharu Saeki*

*RF Semiconductor Development Center, Semiconductor Company, Matsushita Electric Industrial Co., Ltd., Nagaokakyo City, Kyoto, 6178520, Japan

**Device Development Center, Matsushita Electric Industrial Co., Ltd., Kadoma City, Osaka, 5718501, Japan

Abstract ¢ **A very low distortion down converter for a W-CDMA was developed. A LO amplifier is constructed with a differential amplifier and transistors which operate as a push-pull driver amplifier. As this LO amplifier has faster switching time of the differential pair, the down converter achieved a low noise figure (NF) performance. In addition, the low output impedance of the LO amplifier leads to lower supply current without using the LO buffer circuit. Insertion of a resistance between the bases of the transconductance stage of the mixer circuit realized low distortion without a degradation of the noise figure of the down converter. The down converter in SiGe-BiCMOS process achieved conversion gain of 11.0dB, NF of 8.8dB and IIP3 of +3.5dBm with 7.4mA current consumption, 2.8V supply voltage.**

I. Introduction

The third-generation Universal Mobile Telecommunication System (UMTS) is currently being standardized by the third-generation partnership project (3GPP) forum. Using the Wideband Code Division Multiple Access (W-CDMA) technology for the radio interface in Japan and Europe, data rates of up to 2 Mbits/s can be delivered for in-door stationary users and up to 384 kbits/s for wide-area mobile users. One of the most important factor in W-CDMA down converter is 3rd order intermodulation distortion (IMD3) caused by a cross modulation. However, it is difficult to achieve the low distortion and reduce the current consumption at the same time because the low distortion performance needs to have the high current consumption. NF is also the other of the most important factor. But the improvement of the distortion causes the degradation of NF.

This paper presents a very low distortion down converter with low current consumption and low noise figure for W-CDMA systems, using the high performance 0.25um SiGe-BiCMOS process.

II. Down Converter Design

A. LO Amplifier Design

The circuit schematic of LO amplifier for the down converter is shown in Fig. 1. In the LO amplifier, the base of Q1 is connected to the base of Q4, and the base of Q2 is connected to the base of Q3 through capacitors C1 and C2, respectively. Therefore, as the base voltages of Q1 and Q4 operate with common phase and common amplitude mostly, the emitter voltage of Q4 operates with common phase and common amplitude. The base and emitter voltage of Q4 are raised when Q1 is turned on, and Q2 and Q3 are turned off at that time. Therefore, as the current of Q2 becomes lower, the base-emitter voltage (V_{be}) of Q4 is lowered. Consequently, it is compulsorily accelerated the operation of raising the emitter voltage of Q4.

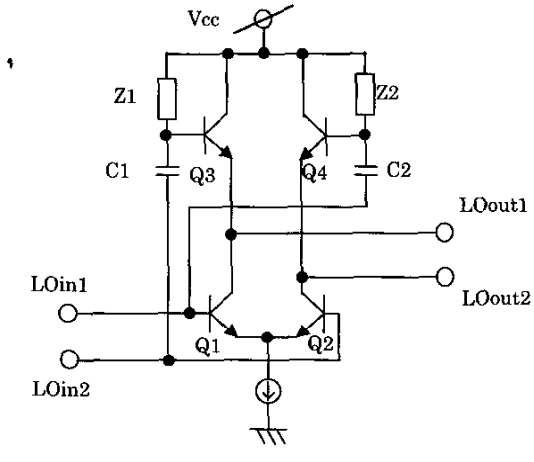

Fig.1 Circuit schematic of the original LO Amplifier

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Adversely, the base and emitter voltage of Q4 are lowered when Q1 is turned off, and Q2 and Q3 are turned on at that time. Therefore, as the current of Q2 becomes higher, the V_{be} of Q4 is raised. Consequently, it is compulsorily accelerated the operation of lowering the emitter voltage of Q4. Thus the shorter switching time is realized. The shorter switching time of the LO amplifier as a push-pull driver gets the lower NF [1].

When Q3 and Q4 operate as an output load, the output impedances are equal to the emitter resistance (***re***) of Q3 and Q4, which are low enough. It is possible to reduce the current consumption without using the LO buffer circuit. Compared to another LO amplifier, which uses spiral inductors, the transistor-loaded (original) LO amplifier can reduce the chip area significantly.

B. Mixer Design

The circuit schematic of a mixer is shown in Fig. 2. Double balanced mixer (DBM) is used because DBM behaves stable and harmonics have the lower output level in compared with Single balanced mixer (SBM). Moreover, to adjust conversion gain and to cancel out the input power level for reducing the IMD3 level in the mixer output, two inductors L1 and L2 are inserted between the emitters of the differential pair and a resistance Z4 is inserted between the bases of the differential pair in the transconductance stage. The good IIP3 characteristics has been achieved by using the mixer and LO amplifier of Fig. 1 and 2.

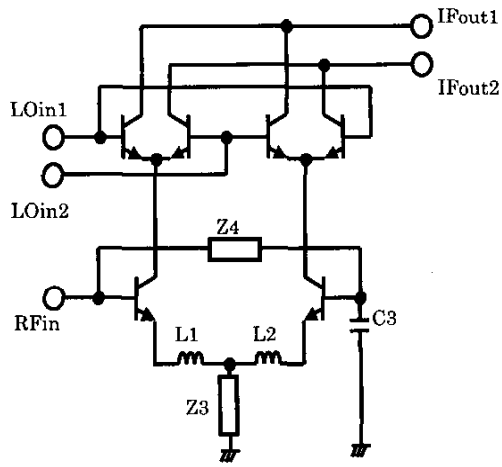


Fig.2 Circuit schematic of the down mixer

Fig.3 shows in the microphotograph of the down converter by using 0.25um SiGe BiCMOS process. The chip area is 2.09x1.7mm^2.

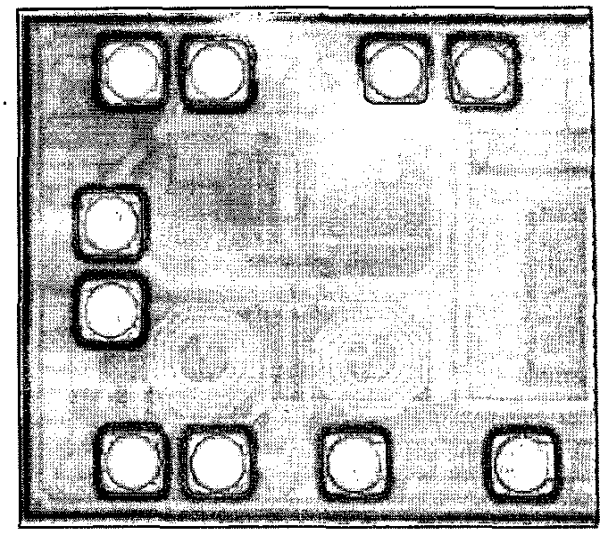
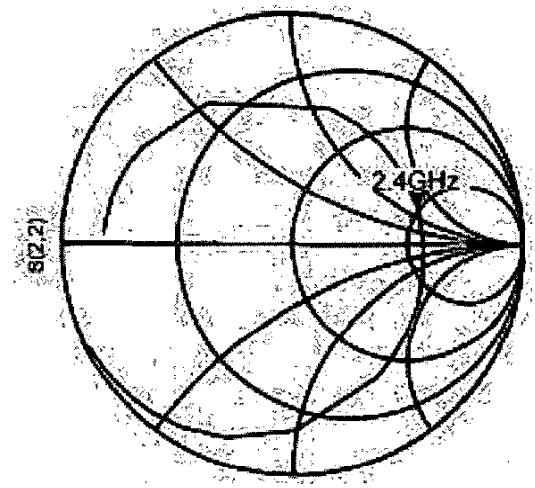


Fig.3 Microphotograph of the down converter

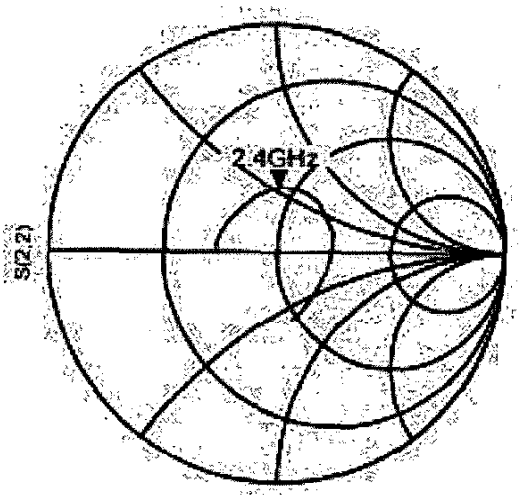
III. Simulation Analysis

The output impedance of the conventional LC-loaded amplifier and the transistor-loaded amplifier (original) are shown in Fig.4.



freq. (100MHz-8GHz)

(a) LC loaded LO amplifier



freq. (100MHz-8GHz)

(b) Transistor loaded LO amplifier (original)

Fig.4 The output S-parameter of the LO amplifier

The output impedance of the transistor-loaded amplifier is very low, compared to the LC-loaded amplifier. Since the output impedance of the transistor-loaded LO amplifier is very low and the transistor-loaded LO amplifier do not need to put the buffer circuit. So the reduction of the current consumption is achieved. And the transistor-loaded LO amplifier has better IIP3 than the LC-loaded LO amplifier as shown in Table I, because the gain of the LC-loaded amplifier is higher than one of the transistor-loaded amplifier as shown in Fig.5.

TABLE I
SIMULATED PERFORMANCE FOR DOWN CONVERTER

	This work	Without resistance	LC type
RF freq.	2.14 GHz	2.14GHz	2.14GHz
Conv. Gain	8.4 dB	10.3 dB	8.3 dB
NF	8.7 dB	6.8 dB	8.9 dB
IIP3	+6.6 dBm	+4.6 dBm	+2.2 dBm
Current	6.7 mA	6.7 mA	7.2 mA

The decrease gain of the LC-loaded amplifier causes the NF degradation. Moreover, insertion of resistance between bases of the differential pair makes IIP3 improvement by 2.0 dB. "Without resistance" in Table I shows the mixer, which has the transistor-loaded LO amplifier and the DBM without the resistance between the bases of the transistor. Compared to "Without resistance", "This work" is improved by 2.0dB IIP3.

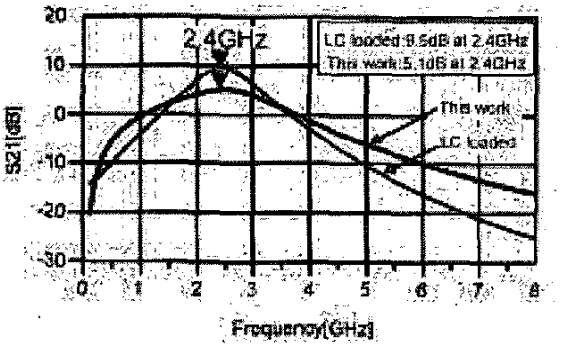


Fig.5 The S21 of the LO amplifier

IV. EXPERIMENTAL RESULTS

The performance of the down converter with LO input frequency at 2.419GHz, input level at -10dBm, and IF output frequency at 279MHz, RF input frequency at 2.11-2.17GHz band with supply voltage of 2.8V is measured. The return loss is lower than 10dB, which means VSWR<2. The result of RF input frequency dependence of conversion gain, NF and IIP3 are shown in Fig. 6.

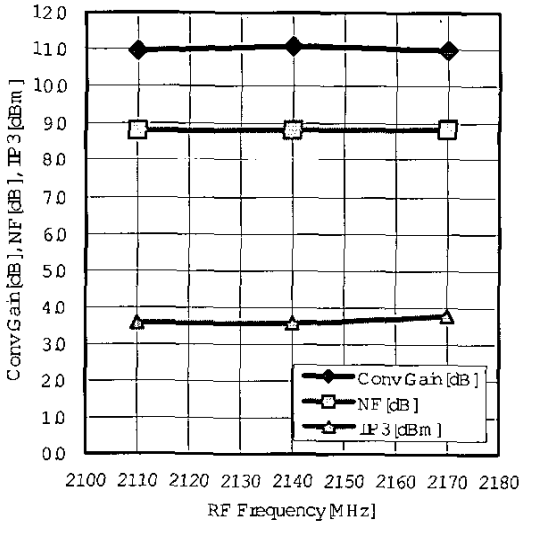


Fig.6 Conversion Gain, NF and IIP3 versus RF frequency

It turns out that characteristic variations are within 0.2dB from 2.11 to 2.17GHz (Fig.6). Measured performances of this down converter are summarized in Table II which comparing with another down converter, which LO amplifier has LC load. The IIP3 of +3.5dBm, the conversion gain of 11.0dB and NF of 8.8dB have been achieved with 7.4mA current consumption. The characteristics of the down converter with LC-loaded LO amplifier has 11.2dB conversion gain, 9.2dB NF and +1.2dBm IIP3 with 7.0mA current consumption.

TABLE II
MEASURED PERFORMANCE FOR DOWN CONVERTER

	This work	LC type
RF freq.	2.14 GHz	2.14GHz
Conv. Gain	11.0 dB	11.2 dB
NF	8.8 dB	9.2 dB
IIP3	+3.5 dBm	+1.2 dBm
Current	7.4 mA	7.0 mA

V. CONCLUSION

The very low distortion down converter for W-CDMA has been developed by using the 0.25um SiGe BiCMOS process. This down converter with original differential push-pull amplifier achieved high IIP3 characteristics of 2.3dB. In addition, the push-pull amplifier realized low supply current without using the LO buffer circuit. NF also has been improved by 0.4 dB.

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